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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,521	04/01/2004	Andrew S. Hildebrant	10031350-1	1566

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/815,521	HILDEBRANT, ANDREW S.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/815,521 filed on 04/01/2004, claims 1-37 are pending.

Claim Objections

2. Claims 2-16, 18, 22-23, 26, 30-31, and 34-37 are objected to because of the following informalities:

as to claims 2 and 18 recites the limitation "said one or more chip defects" in line 2;

as to claims 6 and 22 recites the limitation "said passes simulated good" in line 3;

as to claims 7 and 23 recites the limitation "said one or more chip defects" in line 2;

as to claims 10 and 26 recites the limitation "said one or more chip defects" in line 2;

as to claims 14 and 30 recites the limitation "said passes simulated good" in line; and

as to claims 15 and 31 recites the limitation "said one or more chip defects" in line 2.

There are insufficient antecedent basis for these limitation in the claims.

as to claims 2-16, line 1, before "method" changes "A" to "The".

as to claims 34-37, line 1, before "integrated circuit" changes "An" to "The".

as to claims 5, 9, 25, and 29, line 1, before " comprising the step of", what does applicant mean by the term "first" in the preamble? The recited steps are not limited to a specific order. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 5-7, 10, 13-15, 17-18, 21-23, 26, 29-31, 33-34, and 36-37 rejected under 35 U.S.C. 102(b) as being anticipated by Erle et al. (Erle) (US 6,170,078).

5. **With respect to claims 1 and 17**, Erle discloses a method (col. 1, ll. 5-10) and computer readable storage medium tangibly embodying program instructions (faulty simulation tool code [302]; EDIF code [308], compiler code [306], and behavior model code [304]) (figure 3, col. 4, ll. 26-45) for verifying an integrated circuit device test for testing an integrated circuit device, said comprising the steps of:

simulating a flawed integrated circuit device (faulty device behavior model) comprising one or more known flaws (predetermined faulty behavior) in an integrated circuit device design (col. 1, ll. 55-59, col. 2, ll. 60-63);

simulating a test of said simulated flawed integrated circuit device (col. 1, ll. 48-54, col. 2, ll. 63-65); and

determining whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device (col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6).

6. **With respect to claims 2 and 18**, Erle discloses all the limitation as the forth set of claims, further comprising: modeling said one or more chip defects (faulty device behavior models) with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

7. **With respect to claims 5 and 21**, Erle discloses all the limitation as the forth set of claims, further comprising the first step of: generating said integrated circuit device design that meets specifications of said integrated circuit device (good device behavior model) (fig. 1, element [104], col. 2, ll. 46-47, ll. 58-59).

8. **With respect to claims 6 and 22**, Erle all the limitation as the forth set of claims, further comprising the step of: verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design (fig. 1, element [110], col. 2, l. 67 and col. 3, ll.1-3).

9. **With respect to claims 7 and 23**, Erle discloses all the limitation as the forth set of claims, further comprising: modeling said one or more chip defects (faulty device behavior models) with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

10. **With respect to claims 10 and 26**, Erle discloses all the limitation as the forth set of claims, further comprising: modeling said one or more chip defects (faulty device behavior models) with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

11. **With respect to claims 13 and 29**, Erle discloses all the limitation as the forth set of claims, further comprising the first step of: generating said integrated circuit device design that meets specifications of said integrated circuit device (good device behavior model) (fig. 1, element [104], col. 2, ll. 46-47, ll. 58-59).

12. **With respect to claims 14 and 30**, Erle discloses all the limitation as the forth set of claims, further comprising the step of: verifying that said test passes simulated

good integrated circuit devices of said generated integrated circuit device design (fig. 1, element [110], col. 2, l. 67 and col. 3, ll.1-3).

13. **With respect to claims 15 and 31**, Erle discloses all the limitation as the forth set of claims, further comprising: modeling said one or more chip defects (faulty device behavior models) with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

14. **With respect to claim 33**, Erle discloses an integrated circuit device test verification apparatus, comprising:

an integrated circuit device simulator (figure 1-3) which simulates a flawed integrated circuit device (faulty device behavior model) of an integrated circuit device design (col. 1, ll. 55-59, col. 2, ll. 60-63);

a tester (figure 1-3) simulator which simulates a test executing on an integrated circuit device tester that generates test stimuli (test vector or patterns) (fig. 1, element [102]) and receives test responses (fig. 1, element [110]) (col. 1, ll. 48-54, col. 2, ll. 63-65); and

simulated test results analyzer (fig. 1, element [110]) which determines whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device (col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6).

15. **With respect to claim 34**, Erle discloses the integrated circuit device test verification apparatus in accordance with claim 33, wherein: one or more chip defects

are modeled with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

16. **With respect to claim 36**, Erle discloses the integrated circuit device test verification apparatus in accordance with claim 33, wherein:

said integrated circuit device simulator also simulates a known good integrated circuit device of an integrated circuit device design (fig. 1, element [104]);

said tester simulator simulates said test executing on said integrated circuit device tester (fig. 1, element [110]) (col. 1, ll. 48-54, col. 2, ll. 63-65); and

said simulated test results analyzer determines whether said simulated test of said simulated known good integrated circuit device passes said simulated known good integrated circuit device (col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6).

17. **With respect to claim 37**, Erle discloses the integrated circuit device test verification apparatus in accordance with claim 36, wherein: said simulated test results analyzer determines whether said simulated test of said simulated known good integrated circuit device passes said simulated known good integrated circuit device (col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erle et al. (Erle) (US 6,170,078) in view of Toutounchi et al. (Toutounchi) (US 6,594,610).

20. **With respect to claims 1-32**, Erle discloses a method (col. 1, ll. 5-10) and computer readable storage medium tangibly embodying program instructions (Erle, faulty simulation tool code [302]; EDIF code [308], compiler code [306], and behavior model code [304]) (Erle, figure 3, col. 4, ll. 26-45) for verifying an integrated circuit device test for testing an integrated circuit device, said comprising the steps of:

(claims 1 and 17) simulating a flawed integrated circuit device (faulty device behavior model) comprising one or more known flaws (predetermined faulty behavior) in an integrated circuit device design (Erle, col. 1, ll. 55-59, col. 2, ll. 60-63);

(claims 1 and 17) simulating a test of said simulated flawed integrated circuit device (Erle, col. 1, ll. 48-54, col. 2, ll. 63-65);

(claims 1 and 17) determining whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device (Erle, col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6);

(claims 2, 7, 10, 15, 18, 23, 26, and 31) one or more chip defects are modeled with said one or more known flaws (Erle, fig. 1, elements [106-108], col. 2, ll. 60-63);

(claims 5, 13, 21, and 29) generating said integrated circuit device design that meets specifications of said integrated circuit device (good device behavior model) (fig. 1, element [104], col. 2, ll. 46-47, ll. 58-59);

(claims 6, 14, 22, and 30) verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design (fig. 1, element [110], col. 2, l. 67 and col. 3, ll.1-3);

Erle does not disclose:

(claims 9 and 25) modifying said integrated circuit device design to include said one or more known flaws to generate said flawed integrated circuit device design;

(claims 3-4, 8, 11-12, 16, 19-20, 24, 27-28, and 32) indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

Toutounchi discloses more specifically and more details the limitations Erle already taught, such as (claims 5, 13, 21, and 29) generating said integrated circuit device design that meets specifications of said integrated circuit device (fig. 2, step 122, col. 3, ll. 49-62); and (claims 6, 14, 22, and 30) verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design (Toutounchi, fig. 2, step 124, col. 3, ll. 63-65).

Toutounchi also discloses (claims 3-4, 8, 11-12, 16, 19-20, 24, 27-28, and 32) indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device (Toutounchi, col. 3, ll. 65-67 and col. 4, ll. 1-35); (claims 9 and 25) modifying said integrated circuit device design (reconfiguration or another configuration) to include (introduce fault) said one or

more known flaws to generate said flawed integrated circuit device design (Toutounchi, figure 2, step 128, col. 3, ll. 65-67, col. 4, ll. 19-25);

It would have been obvious to one of ordinary skill in the art to combine Erle and Toutounchi teachings for performed a faulty test (Erle, col. 1, ll. 5-10 and Toutounchi, col. 1, ll. 5-10) of using at least one faulty device behavior model associated with predetermined (known) defects for simulating faulty circuit design to detect the predetermined defect (Erle, col. 3, ll. 1-6 and Toutounchi, col. 4, ll. 15-18). However, if the predetermined defects that are not caught, modified the configuration of circuit design (Toutounchi, col. 4, ll. 19-25) or the set of test vector (pattern) (Toutounchi, col. 4, ll. 30-35) until all the faults are coverage.

21. **With respect to claims 33-37**, Erle disclose an integrated circuit device test verification apparatus comprising:

(claims 33 and 36) an integrated circuit device simulator (figure 1-3) which simulates a flawed integrated circuit device (faulty device behavior model) of an integrated circuit device design (col. 1, ll. 55-59, col. 2, ll. 60-63);

(claims 33 and 36) a tester (figure 1-3) simulator which simulates a test executing on an integrated circuit device tester that generates test stimuli (test vector or patterns) (fig. 1, element [102]) and receives test responses (fig. 1, element [110]) (col. 1, ll. 48-54, col. 2, ll. 63-65); and

(claims 33 and 36-37) simulated test results analyzer (fig. 1, element [110]) which determines whether said simulated test of said simulated flawed integrated circuit

device discovered said one or more known flaws in said flawed integrated circuit device (col. 1, ll. 65-67, col. 2, ll. 1-4, ll. 65-67 and col. 3, ll. 1-6).

(claims 34) one or more chip defects are modeled with said one or more known flaws (fig. 1, elements [106-108], col. 2, ll. 60-63).

Erle does not discloses (claim 35) indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

Toutounchi discloses indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device (Toutounchi, col. 3, ll. 65-67 and col. 4, ll. 1-35).

It would have been obvious to one of ordinary skill in the art to combine Erle and Toutounchi teachings for performed a faulty test (Erle, col. 1, ll. 5-10 and Toutounchi, col. 1, ll. 5-10) of using at least one faulty device behavior model associated with predetermined (known) defect for simulating faulty circuit design to detect the predetermined defect (Erle, col. 3, ll. 1-6 and Toutounchi, col. 4, ll. 15-18). However, if the predetermined defects that are not caught, modified the configuration of circuit design (Toutounchi, col. 4, ll. 19-25) or the set of test vector (pattern) (Toutounchi, col. 4, ll. 30-35) until all the faults are coverage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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